FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: PD990014

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/936479

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/02182	13March2000(13.03.00)	25March1999(25.03.99)

TITLE OF INVENTION: METHOD FOR THE MANAGEMENT OF DATA RECEIVED VIA A DATA BUS, AND APPARATUS FOR CARRYING OUT THE METHOD

APPLICANT(S) FOR DO/EO/US: Siegfried Schweidler, Timothy Heighway, Klaus Gaedke

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210). Attached to Item 13
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. with references attached
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail 20. Return postcard receipt
20. ~~☐ Other items or information:~~

CERTIFICATE OF MAILING UNDER 37 CFR 1.10

"Express Mail" mailing no.	Date of Deposit
EL685391650US	September 13, 2001

I hereby certify that this application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Typed or printed name of person mailing application	Signature of person mailing application
Davida Fornarotto	Davida Fornarotto

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/936479	PCT/EP00/02182	PD990014

531 Rec'd PC 13 SEP 2001

21. The following fees are submitted:	CALCULATIONS PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :	
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO $1000.00	
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO $860.00	
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00	
☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =	860.00
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total claims	9 - 20 =	0	x $18.00	
Independent claims	1 - 3 =	0	x $80.00	
Multiple Dependent Claims (check if applicable).			☐	

TOTAL OF ABOVE CALCULATIONS =	860.00	
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SUBTOTAL =	860.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +		
TOTAL NATIONAL FEE =	860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable). ☐	40.00	
TOTAL FEES ENCLOSED =	900.00	
Amount to be: refunded		$
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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Mr. Joseph S. Tripoli
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SEP 17 2001
PCT INITIAL PROCESSING

Paul P. Kiel
SIGNATURE

Paul P. Kiel
NAME

40,677
REGISTRATION NUMBER

9/13/01
DATE

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EXPRESS MAIL LABEL NO. EL685391650US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Siegfried Schweidler, Timothy Heighway, Klaus Gaedke

Filed : Herewith

For : METHOD FOR THE MANAGEMENT OF DATA RECEIVED VIA A DATA BUS, AND APPARATUS FOR CARRYING OUT THE METHOD

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Sir:

In the US national phase application of PCT/EP00/02182 filed herewith, please enter the following amendments:

IN THE SPECIFICATION:

Please amend the specification as follows:

On Page 1, line 3, insert the following paragraph:

-- This application claims the benefit of German serial no. 19913585.1 filed March 25, 1999 which is hereby incorporated herein by reference, and which claims the benefit under 35 U.S.C. § 365 of International Application PCT/EP00/02182, filed March 13, 2000, which was published in accordance with PCT Article 21(2) on October 5, 2000 in English.--

IN THE CLAIMS:

Please amend the claims as follows. A marked-up version of the amended claims is attached herewith.

1. Method for the management of data received via a data bus, the data being transmitted in bus packets having a variable length, the data being divided into data blocks having a defined length, a combination of a defined number n of data blocks forming a data source packet, section-by-section transmission of the data source packet within the framework of data blocks being permitted, wherein modulo-n counting of the data blocks is carried out in order to determine the data source packet boundaries, and in that the beginning of a new data source packet is signaled to a memory management device at the beginning of the next counting interval.

2. Method according to Claim 1, wherein each bus packet is subjected to CRC checking and the checking results are buffer-stored in order to be able to ascertain whether a data source packet transmitted in two or more bus packets has been transmitted without any errors.

3. Method according to Claim 1 wherein a reference counter reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data blocks is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal is output in the event of non-correspondence.

4. Method according to Claim 1, wherein the defined number n of data blocks of a data source packet corresponds to the number 8 and the modulo-n counting is correspondingly modulo-8 counting.

5. Apparatus for carrying out the method according to Claim 1, having a memory unit to which the received data are written in order, and having a memory management device wherein a modulo-n counter is provided, which counts the received data

blocks and outputs a data source packet start signal to the memory management device at the beginning of the next counting interval.

6. Apparatus according to Claim 5, further comprising a CRC checking unit, by means of which the data in the received bus packets are checked with regard to freedom from errors, where the checking results of a plurality of successive bus packets are buffer-stored and combined if the data source packet start signal has been identified, and where the CRC checking unit outputs an error signal if one of the combined checking results includes an identified error.

7. Apparatus according to Claim 5, further comprising a data block reference counter, which effects the comparison counting of the received data blocks, and where comparison means are provided which compare the counter reading of the data block reference counter with the received reference counter reading of the bus packet and output an error signal in the event of non-correspondence.

8. Apparatus according to Claim 1, further comprising a data counter, by which the data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been counted are as many as are defined as belonging to a data block.

9. Apparatus according to Claim 1, wherein the data bus is designed according to the IEEE 1394 standard and the apparatus is part of a data link layer module in the interface for this data bus.

IN THE ABSTRACT:

Please add the following Abstract.

-- The format of the transmission of isochronous data packets via the IEEE 1394 bus is defined in the IEC 61883 Standard. In this case, it is possible to use an operating mode in which the same number of data blocks is always transmitted in a bus packet. In this case, the memory management is extremely simple and the data source packet boundaries can easily be determined. However, the IEC 61883 standard also leaves open the possibility of transmitting a variable number of data blocks in the

context of isochronous data transmission with the aid of bus packets. In this case, however, subsequently ascertaining the data source packet boundaries poses a problem. The invention specifies a solution, favourable in terms of outlay, as to how the data source packet boundaries can easily be reconstructed. It is based essentially on modulo-n counting of data blocks.--

REMARKS

The specification has been amended to include a reference to the priority applications.

The claims have been amended to remove reference indicia and to meet the requirements of the United States.

To meet the requirements of the United States, the Abstract (as originally filed in the PCT application) is added.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832

Respectfully submitted,
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September 13, 2001

MARKED UP VERSION OF THE CLAIMS

1.(AMENDED) Method for the management of data received via a data bus, the data being transmitted in bus packets having a variable length, the data being divided into data blocks [(DB0-DB7)] having a defined length, a combination of a defined number n of data blocks [(DB0-DB7)] forming a data source packet [(SP0-SP2)], section-by-section transmission of the data source packet [(SP0-SP2)] within the framework of data blocks being permitted, [**characterized in that**] wherein modulo-n counting of the data blocks [(DB0-DB7)] is carried out in order to determine the data source packet boundaries, and in that the beginning of a new data source packet [(SP1, SP2)] is signaled to a memory management device [(31)] at the beginning of the next counting interval.

2.(AMENDED) Method according to Claim 1, [in which] wherein each bus packet is subjected to CRC checking and the checking results are buffer-stored in order to be able to ascertain whether a data source packet [(SP0-SP2)] transmitted in two or more bus packets has been transmitted without any errors.

3.(AMENDED) Method according to Claim 1 [or 2, in which] wherein a reference counter reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data blocks [(DB0-DB7)] is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal [(DBC_ERR)] is output in the event of non-correspondence.

4.(AMENDED) Method according to [one of the preceding claims, in which] Claim 1, wherein the defined number n of data blocks [(DB0-DB7)] of a data source packet [(SP0-SP2)] corresponds to the number 8 and the modulo-n counting is correspondingly modulo-8 counting.

5.(AMENDED) Apparatus for carrying out the method according to [one of the preceding claims] Claim 1, having a memory unit [(30)] to which the received data are written in order, and having a memory management device [(31), **characterized**

in that] wherein a modulo-n counter [(33)] is provided, which counts the received data blocks [(DB0-DB7)] and outputs a data source packet start signal [(SP_ST)] to the memory management device [(31)] at the beginning of the next counting interval.

6.(AMENDED) Apparatus according to Claim 5, [which furthermore has] further comprising a CRC checking unit [(32)], by means of which the data in the received bus packets are checked with regard to freedom from errors, where the checking results of a plurality of successive bus packets are buffer-stored and combined if the data source packet start signal [(SP_ST)] has been identified, and where the CRC checking unit [(32)] outputs an error signal [(CRC_ERR)] if one of the combined checking results includes an identified error.

7.(AMENDED) Apparatus according to Claim 5 [or 6, which furthermore has] , further comprising a data block reference counter [(34)], which effects the comparison counting of the received data blocks [(DB0-DB7)], and where comparison means are provided which compare the counter reading of the data block reference counter [(34)] with the received reference counter reading of the bus packet and output an error signal [(DBC_ERR)] in the event of non-correspondence.

8.(AMENDED) Apparatus according to [one of the preceding claims, which furthermore has] Claim 1, further comprising a data counter [(35)], by which the data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been counted are as many as are defined as belonging to a data block [(DB0-DB7)].

9.(AMENDED) Apparatus according to [one of the preceding claims, where] Claim 1, wherein the data bus is designed according to the IEEE 1394 standard and the apparatus is part of a data link layer module in the interface for this data bus.

Method for the management of data received via a data bus, and apparatus for carrying out the method

The invention relates to a method for the management of data received via a data bus. The method can expediently be employed in particular when isochronous data packets are being received. The invention furthermore relates to an apparatus for carrying out the method. The apparatus may be, in particular, part of a bus interface for the connected data bus.

Prior art

The invention is based on a method for the management of data packets received via the data bus of the generic type of the independent Claim 1. For quite a long time now the convergence of the product sectors of consumer electronics (hifi, video, audio) and personal computing has been trumpeted under the catchword multimedia and has actually been propelled by many manufacturers from both camps. The merging of the two product sectors means that work concerned with the subject of data exchange between the equipment of the different product sectors or else between the equipment within one product sector is becoming more and more significant. This is also apparent from the efforts for standardization with regard to this subject, which are already well advanced. Specifically, the so-called IEEE 1394 serial bus already provides an internationally standardized and very widely accepted bus for data exchange between terminals from both product groups. The precise designation of the aforementioned standard is: IEEE Standard for high performance serial bus, (IEEE) STD 1394-1995, IEEE New York, August 1996.

The invention that is to be described here is concerned with the so-called isochronous data transfer within the abovementioned bus system. In this connection, isochronous means that data to be transmitted arise

regularly at a data source, the data also arising with approximately the same size each time. Examples of such data sources are video recorders or camcorders, audio devices such as CD players or DAT recorders, and also DVD players or videophone devices, etc. An international standard has been specially developed for this application of isochronous data transmission. The precise designation of this standard is: IEC International Standard 61883 "Consumer Audio/Video Equipment-Digital Interface, 1st edition 1998". The first part of this standard describes the general data packet format, the data flow management and the connection management for audiovisual data. General transmission rules for control commands are likewise defined.

A very frequent application relates to the transmission of MPEG2-coded video or audio data. The data are transported via the bus in packets, as already mentioned. In this case, the following structure is provided in the abovementioned Standard IEC 61883: the data generated in the data source are divided into so-called data source packets having a defined size. For MPEG2 video data transmission, for example, the standard stipulates that a data source packet is composed for example of 8 data blocks of identical size. In this case, the data block size can be programmed. It may be between one and 256 quadlets, where a quadlet corresponds to a combination of 4 data bytes. According to the Standard, the data source packets can be transmitted such that they are combined in a single bus packet. In this case, no addressing problem is manifested in the device that has received the data, because it is always clear that, for each new received bus packet, a completely received data source packet has arrived.

However, the abovementioned standard also certainly permits another mode, in which fewer than eight data blocks can be transmitted in a bus packet. Put in concrete terms, it is also possible to transmit so-called dummy packets which do not contain any data blocks at

all. However, further possible numbers of data blocks in a bus packet of between 0 and 8 are also allowed. The invention is now concerned with the concrete realization of this more general transmission mode.

Invention

The following problem arises in the realization of the general transmission mode. If it happens on an occasion that a bus packet contains fewer than eight data blocks of useful data, a complete data source packet can no longer be transmitted in the bus packet. Consequently, data blocks of the data source packet also follow in the next bus packet. If eight data blocks are then transmitted again e.g. in the next bus packet, the data block boundary between two data source packets is no longer synchronous with the end of the bus packet but rather lies somewhere in the bus packet. The memory management unit in the receiver device has to search for this boundary since it has to provide the information of where a data source packet starts and ends in special registers. This is necessary in order that it can make the data available to the application process after reception source packet by source packet. Thus, it is necessary to find a solution as to how the start and the end of a data source packet transmitted in fragments can subsequently be ascertained in the receiver device.

The invention achieves this object in such a way that it carries out modulo-n counting of the data blocks and signals the beginning of a new data source packet at the beginning of the respective next time interval of modulo-n counting. For the special case of the transmission of MPEG 2 source data, where the data source packet in each case comprises eight data blocks, modulo-8 counting is correspondingly carried out. In other words, the counting interval begins at the counter reading 0 and ends at the counter reading 7. Afterwards, the next counting interval then follows again, beginning with the counter reading 0.

Further improvements of the method are possible by virtue of the measures evinced in the dependent claims. Since, according to the IEEE 1394 Standard, each bus packet must be subjected to CRC checking, it is expedient to buffer-store the checking results of successive bus packets. It is ensured that the data are free from errors only when all the bus packets containing a data block of the data source packet have been able to be subjected to CRC checking without a complaint. In the event of a complaint, a CRC error signal can then be output. The entire data source packet can then not be forwarded to the application process.

Checking the completeness of the transmitted data with the aid of a reference counter reading provided in each bus packet can be done as follows: comparison counting of the received data blocks is effected and each time the specific data block with which the reference counter reading is associated is received, a comparison is made between the reference counter reading and the result of the comparison counting and an error signal is output in the event of non-correspondence. The IEC 61883 Standard stipulates that a DBC reference value which is valid for the first subsequent data block is entered in each bus packet. By counting the received data blocks and comparing the result with the received reference value, it is thus possible easily to ascertain whether e.g. a whole bus packet has not been received. The error monitoring is again improved by this measure.

The following measures, which specify the way in which the corresponding object of the invention is achieved, are advantageous for an apparatus for carrying out the method according to the invention. The apparatus firstly comprises a memory unit to which the received data are written in order. Furthermore, a memory management device is provided which prescribes, in particular, the addresses for the read-in and read-out process. What are then essential are the modulo-n counter, by which the received data blocks are counted

up, and the generation of the data source packet start signal when the modulo-n counter begins a new counting interval. The data source packet start signal is forwarded to the memory management device, which can then make a corresponding entry in a special register. These measures are specified in Claim 5.

Further advantageous measures for the apparatus according to the invention are also contained in the dependent Claims 6-8.

Drawings

Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the description below. In the figures:

Figure 1 shows the structure of a plurality of successive bus packets for the general transmission mode, and

Figure 2 shows a block diagram of the apparatus according to the invention.

Exemplary embodiments of the invention

Figure 1 shows an exemplary sequence of transmitted bus packets. The first transmitted bus packet is illustrated at the top in Figure 1 and the last transmitted bus packet is correspondingly illustrated at the bottom in Figure 1. The precise structure of a bus packet for isochronous data transmission is specified in the abovementioned IEC 61883 Standard. For the disclosure of the invention, therefore, reference is also expressly made to this standard.

In Figure 1, the reference numeral 10 designates the header of the bus packet. It contains the details regarding the data field of the isochronous data packet, to be precise in a number of bytes and also further information, but this need not be discussed in any more detail below. The header 10 of the bus packet is followed by a data field. The latter extends through the areas 11-15, referring to the first bus packet illustrated. At the

end of the bus packet there also follows an area 16, in which a CRC check word is stored. A so-called CIP header is always provided at the beginning of the data field of a bus packet. CIP is the abbreviation of "common isochronous packet". The CIP header contains a series of information items which describe the isochronous data transfer. Thus, e.g. an identification number SID for the data source is contained therein. Furthermore, it stipulates the size of the subsequent data blocks in the bus packet. Likewise, a detail FN (fraction number) is also contained, which specifies the number of data blocks into which a data source packet is divided. As already mentioned, there are always 8 data blocks per data source packet in the case of MPEG 2 video data. A further detail QPC (quadlet padding count) relates to how many padding quadlets are attached to the end of the data source packet in order to guarantee that the latter is divided into data blocks of the same size. Furthermore, an information item SPH (source packet header) is provided, which specifies whether a header for the data source packet is likewise also provided in the bus packet. Furthermore, a DBC value (data block counter) is also provided. This value specifies which data block is the first data block in the bus packet. Therefore, all the data blocks are consecutively numbered individually. This value practically constitutes a reference counter reading which can easily be used to check whether a bus packet has not been received. To that end, the received data blocks are all counted up in the receiver station. Each time a new bus packet is received, the DBC value contained therein is compared with the counted comparison value. Only if both values correspond have all the data blocks been received and no bus packet has been lost. Further information items in the CIP header include an FMT entry (format ID). This entry can be used to signal that the bus packet contains no data at all and is a so-called dummy packet. An FDF entry (format dependent field) may also be defined, this being mentioned only for

the sake of completeness, and also an SYT entry, which comprises a time specification for the bus packet. The data blocks for the first data source packet SP0 then follow in the subsequent areas 12, 13, 14 and 15. The data blocks are individually consecutively numbered from DB0-DB3. The entry 0 in the data area 11 is intended to indicate that the DBC value for this first bus packet is set to the value 0, which is synonymous with the fact that the first data block in this bus packet has the number 0. This must, of course, also be taken into consideration for the comparison counting. Therefore, the comparison count begins at 0. The next bus packet contains a total of 8 data blocks. They reside in the data fields 12-15 and 17 to 20. The data blocks DB4 to DB7 of the data source packet SP0 are additionally contained in this second bus packet. There then follow the data blocks DB0 to DB3 of the data source packet SP1. The detail 4 in the data field 11 indicates that the 4th data block of the isochronous data transmission can be found in this bus packet. In the third bus packet, there then additionally follow in the data fields 12, 13, 14, 15, 17, 18 the outstanding data blocks DB4 to DB7 of the second data source packet and the first two data blocks of the next data source packet SP2. Thus, this bus packet contains a total of six data blocks. The detail 12 in the data field 11 again corresponds to the DBC value of this bus packet. It means that the data block that follows first in this bus packet is the twelfth data block of the isochronous transmission. In the fourth bus packet, there then additionally follow the remaining data blocks of the data source packet SP2, namely DB2 to DB7. The DBC value in the data field 11 of this bus packet is correspondingly 18.

The boundary between the data blocks of the first data source packet SP0 and the data blocks of the second data source packet SP1 is situated in the middle of the second bus packet. The boundary between the data blocks of the second bus packet SP1 and the data blocks of the

third bus packet SP2 is situated in the last third of the third bus packet. These boundaries must be determined in order that the corresponding address entries can be made in the special registers of the memory management unit.

The invention affords a solution enabling the data source packet boundaries to be determined; this solution is explained in more detail below with reference to Figure 2. Figure 2 shows the components relevant to the invention. These components are parts of a data link layer circuit of an IEEE 1394 bus interface. The reference number 30) designates a memory unit which is provided below for receiving and buffer-storing data. It may be part of a larger memory unit, just a specific area within the larger memory simply being allocated for this purpose. The received data pass via the bus 37 to the memory unit 30. The data are buffer-stored in the memory unit 30 until they are forwarded to the application unit. In this case, the data are output likewise via the bus 37 to the application unit, which is not specifically illustrated in Figure 2. The following units also have access to the memory unit 30: CRC checking unit 32, modulo-8 counter 33, DB counter 34, data counter 35 and evaluation logic unit 36. All of these units are connected to one another via an internal bus 38 and are likewise connected to the memory unit 39 as well. The memory management unit 31 is also a further separate unit. The said memory management unit likewise has access to the memory unit 30 via the internal bus 38. Therefore, it also serves as the bus master for the internal bus 38 and allocates it to the individual connected units. It is connected to the memory unit 30 via a separate bus 39. Moreover, a bus 40 is connected to the memory management unit 31, via which bus control data are exchanged with the external application unit. Separate control lines additionally lead from the evaluation unit 36 to the memory management unit 31. These lines are firstly a line 41 via which a data source packet start signal SP_ST is transmitted, secondly a line 42 via which an error signal

DBC_ERR is output, and thirdly a line 43 via which a CRC error signal CRC_ERR is output.

In order now to find the data source packet boundaries, the apparatus described operates as follows: the individual data blocks, which after all have a constant size, are counted in the modulo-8 counter 31. If this counter starts to count with the counter reading 0, it will reach its highest value, referring to the example of Figure 1, at the last data block DB7 of the data source packet SP0 and then start at 0 again after the last data block DB7 has been completely written to the memory. It then outputs the data source packet start signal SP_ST to the memory management unit 31, which then transfers the address that is now valid for the new data into the corresponding special register for the beginning of the next data packet. Since the data blocks all have the same size, there is no need to provide a special register in which the end address of the last data packet of a data source packet has to be entered.

Since the modulo-8 counter sets the counter reading to 0 again and then continues to count, it will have reached the counter reading 7 precisely again after the data block DB7 of the data source packet SP1 has been written in. It will therefore output a data source packet start signal which is forwarded via the evaluation unit 36 to the memory management unit 31 and causes the latter to store the memory address in the further special register. The counting is begun at 0 again and a data source packet start signal SP_ST would be generated anew after the reception of the data block DB7 of the data source packet SP2.

To ensure, however, that the data source packet start signals that are generated actually lead to the transfer of the corresponding address in the special registers, it is a precondition in this exemplary embodiment that error signals are not simultaneously present on the lines 42, 43. This is because otherwise the received data have been detected as containing errors

and they are no longer allowed to be passed on to the application unit. Each received bus packet is checked with regard to freedom from errors in the CRC checking unit 32. Since the CRC check word at the end of each bus packet in the data field 16 only relates to all the data in this bus packet, the fact that a data source packet is free from errors can only be ascertained such that the CRC checking results of the individual bus packets are collected and are jointly evaluated each time the data source packet start signal is generated. If one of the CRC check words of the bus packets that are considered together indicates an error, the error signal CRC_ERR is output via the line 43. For example, after the generation of the data source packet start signal after the reception of the data block DB7 of the first data source packet SP0, the two CRC checking results for the first received bus packet and also for the second received bus packet must indicate freedom from errors in order that no error signal is output via the line 43. As already mentioned, the CRC checking of the individual bus packets is done in the CRC checking unit 32. The collection of the individual checking results is then done in the evaluation unit 36. The same is true with regard to the generation of the error signal CRC_ERR when one of the checking results concerning a data source packet indicates an error.

The DB counter 34 counts up all the received data blocks. According to the IEC 61883 Standard, this counter is an 8-bit counter. If all the bus packets are received properly, this counter will respectively have the counter readings 4, 12 and 18 after the reception of the first, second and third data packets. These values are indeed also entered as reference values in the data fields 11 of the bus packets 2, 3 and 4. However, should the counter not have the counter reading as respectively specified in the data field 11, the evaluation unit 36 will generate the error signal DBC_ERR already mentioned.

The data counter 35 operates as follows: it counts the data in units of bytes. In the IEC 61883 Standard, the data block size is specified in units of quadlets. The data block size can be programmed; to be precise all values between 1 and 256 quadlets are possible. The stipulated value is contained in the CIP header CIPH. This value is evaluated and is then available in the evaluation logic unit 36. The data counter 35 is then set in such a way that, when the end of a data block is reached, the said data counter generates a data block counting pulse and outputs it to the data block counter 34.

Various adaptations and modifications of the exemplary embodiments described are possible. The structure with the various internal bus lines and bus lines provided for the external components, as described, may be chosen differently. Parts of the apparatus explained may also be realized by software. The invention is not restricted to use with the IEEE 1394 bus mentioned. It can also be used for other wire-based bus systems or else for wire-free bus systems.

Patent Claims

1. Method for the management of data received via a data bus, the data being transmitted in bus packets having a variable length, the data being divided into data blocks (DB0-DB7) having a defined length, a combination of a defined number n of data blocks (DB0-DB7) forming a data source packet (SP0-SP2), section-by-section transmission of the data source packet (SP0-SP2) within the framework of data blocks being permitted, **characterized in that** modulo-n counting of the data blocks (DB0-DB7) is carried out in order to determine the data source packet boundaries, and in that the beginning of a new data source packet (SP1, SP2) is signalled to a memory management device (31) at the beginning of the next counting interval.

2. Method according to Claim 1, in which each bus packet is subjected to CRC checking and the checking results are buffer-stored in order to be able to ascertain whether a data source packet (SP0-SP2) transmitted in two or more bus packets has been transmitted without any errors.

3. Method according to Claim 1 or 2, in which a reference counter reading is transmitted in each bus packet in order to check the completeness of the transmitted data, and in which comparison counting of the received data blocks (DB0-DB7) is effected and, when the data block associated with the reference counter reading is received, the result of the comparison counting is compared with the reference counter reading and an error signal (DBC_ERR) is output in the event of non-correspondence.

4. Method according to one of the preceding claims, in which the defined number n of data blocks (DB0-DB7) of a data source packet (SP0-SP2) corresponds to the number

8 and the modulo-n counting is correspondingly modulo-8 counting.

5. Apparatus for carrying out the method according to one of the preceding claims, having a memory unit (30) to which the received data are written in order, and having a memory management device (31), **characterized in that** a modulo-n counter (33) is provided, which counts the received data blocks (DB0-DB7) and outputs a data source packet start signal (SP_ST) to the memory management device (31) at the beginning of the next counting interval.

6. Apparatus according to Claim 5, which furthermore has a CRC checking unit (32), by means of which the data in the received bus packets are checked with regard to freedom from errors, where the checking results of a plurality of successive bus packets are buffer-stored and combined if the data source packet start signal (SP_ST) has been identified, and where the CRC checking unit (32) outputs an error signal (CRC_ERR) if one of the combined checking results includes an identified error.

7. Apparatus according to Claim 5 or 6, which furthermore has a data block reference counter (34), which effects the comparison counting of the received data blocks (DB0-DB7), and where comparison means are provided which compare the counter reading of the data block reference counter (34) with the received reference counter reading of the bus packet and output an error signal (DBC_ERR) in the event of non-correspondence.

8. Apparatus according to one of the preceding claims, which furthermore has a data counter (35), by which the data are counted in particular in units of bytes and which outputs a data block counting signal if the number of data that have been counted are as many as are defined as belonging to a data block (DB0-DB7).

9. Apparatus according to one of the preceding claims, where the data bus is designed according to the IEEE 1394 standard and the apparatus is part of a data link layer module in the interface for this data bus.

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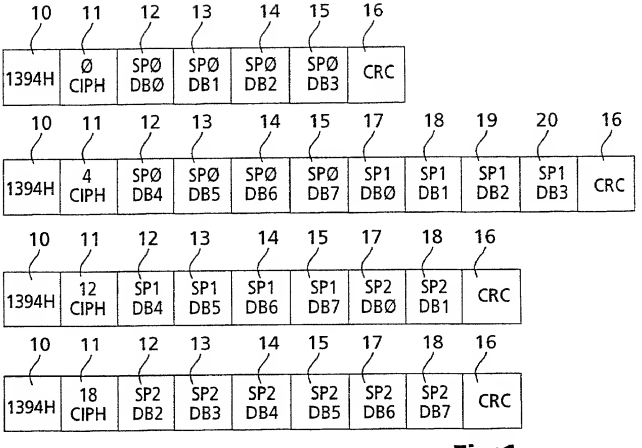
10 11 12 13 14 15 16
1394H Ø CIPH SPØ DBØ SPØ DB1 SPØ DB2 SPØ DB3 CRC
10 11 12 13 14 15 17 18 19 20 16
1394H 4 CIPH SPØ DB4 SPØ DB5 SPØ DB6 SPØ DB7 SP1 DBØ SP1 DB1 SP1 DB2 SP1 DB3 CRC
10 11 12 13 14 15 17 18 16
1394H 12 CIPH SP1 DB4 SP1 DB5 SP1 DB6 SP1 DB7 SP2 DBØ SP2 DB1 CRC
10 11 12 13 14 15 17 18 16
1394H 18 CIPH SP2 DB2 SP2 DB3 SP2 DB4 SP2 DB5 SP2 DB6 SP2 DB7 CRC

Fig.1

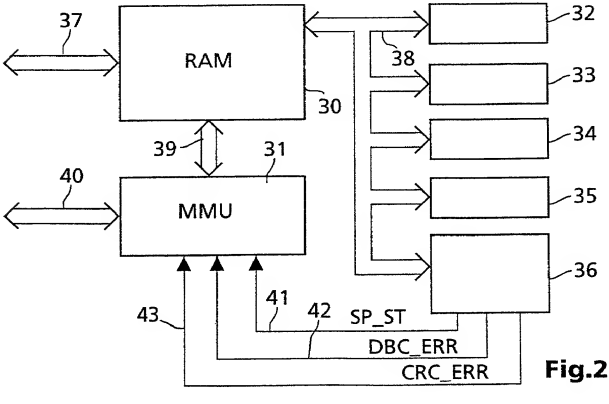
37
RAM
30
38
32
33
34
35
36
39
31
40
MMU
41
42
43
SP_ST
DBC_ERR
CRC_ERR

Fig.2

DECLARATION FOR UNITED STATES PATENT APPLICATION,
POWER OF ATTORNEY, DESIGNATION OF CORRESPONDENCE ADDRESS

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR THE MANAGEMENT OF DATA RECEIVED VIA A DATA BUS, AND APPARATUS FOR CARRYING OUT THE METHOD

the specification of which

(CHECK ONE) ( ) is attached hereto.

(xx) was filed on March 13, 2000, Application Serial. No. PCT/EP 00/02182 and was amended on .

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

I hereby claim foreign priority benefits under 35 USC 119 of any foreign application(s) for patent, utility model, design or inventor's certificate having a filing date before that of the application(s) on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Date Filed	Yes	No
19913585.1	DE	March 25, 1999	xx	

I hereby claim the benefit under 35 USC 120 of any US Application(s) listed below, and, insofar as the subject matter of each of the claims of this Application is not disclosed in the prior US application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 CFR 1.56(a).

Serial No.: Filed:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under of 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Joseph S. Tripoli (Reg. No. 26,040) Telephone: (609) 734-9443.

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